REMARKS

We have carefully considered the Office Action dated November 1, 2005, in which all claims are rejected as obvious over United States Patent 5,452,429 to Fuoco et al. In response to the Office Action, we have amended the independent claims, to more particularly point out the current invention. Further, we have amended claim 8 to overcome a section 112 rejection and similarly amended claim 11, which also contains the referenced language.

The current system utilizes an error correction code that provides, in its syndrome, an indication of both the buffer memory location of a data word and the location(s) within the data word of one or more erroneous bits. The current system encodes the data as a plurality of data words and produces a set of parity check bits that apply to all of the data. The data are stored in respective buffer memory locations and the parity check bits are stored in a separate buffer memory location, e.g., the location that follows the locations in which the data are stored. See, Fig. 3 of the current application.

The generator matrix used to produce the parity check bits contains a data portion and a parity check generation portion. The parity check generation portion comprises rows of bits that correspond to binary representations of the buffer locations to be used to store the data. When the data and parity check bits are read from the buffer memory, the system regenerates the parity check bits and, using the read-back and regenerated parity check bits, produces a result, or syndrome, that is usable to directly identify which of the

data words contains an error by identifying the buffer location that contains the data word. The result is also usable to identify the locations of the erroneous bits within the data code word contained in the indentified buffer location.

As discussed beginning on page 18 of the application, particular bits of the syndrome, in the example, bits S[4]-S[13] indicate an address offset that points to the buffer location of the particular data word that contains the error, and the bits S[0]-S[3] are usable to identify a bit location within the data code word that is contained in the indicated memory location. The remaining bits S[14] and S[15] are a two-bit syndrome code that signals whether a single or double bit error has been detected. In the example discussed beginning at page 18, one bit errors are corrected and double-bit errors are flagged. In other examples, two bit errors are corrected.

The Fuoco reference describes a system in which a given memory location in an add-on memory contains **both** data and the corresponding parity check bits. In the example described in the Fuoco patent, the memory location is 40 bits wide and a data word consists of a four byte string. The memory location contains the four byte string or 32 bits of data, and the seven parity check bits that correspond to the string. The 40th bit of the memory location is a flag. See, Col. 3, lines 28-34; Col. 4, lines 6-9. Accordingly, with the parity check bits stored in the **same** memory location as the data to which they correspond, there is no need in the Fuoco system to generate or use parity check bits which produce a result, or syndrome, that can be used to identify the buffer location in which is stored a data word with one or more erroneous bits.

Thus, the Fuoco reference does not teach or suggest the current invention because, *inter alia*, the Fuoco reference does not teach or suggest a method or apparatus for generating and using parity check bits that are stored in a separate buffer location from the data; and further, the Fuoco reference does not teach or suggest generating or using parity check bits that produce a result that is usable to directly identify the buffer location that contains a data word with one or more erroneous bits and the locations of the erroneous bits within the data word, as set forth in the amended independent claims and the claims that depend therefrom.

In light of the above, we respectfully request that the Examiner reconsider the rejection of the claims and issue a Notice of Allowance for all pending claims.

Please charge any fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

Patricia A. Sheehan
Reg. No. 32,301
CESARI AND MCKENNA, LLP
88 Black Falcon Avenue
Boston, MA 02210-2414
(617) 951-2500